Flexible One Diode-One Phase Change Memory Array Enabled by Block Copolymer Self-Assembly

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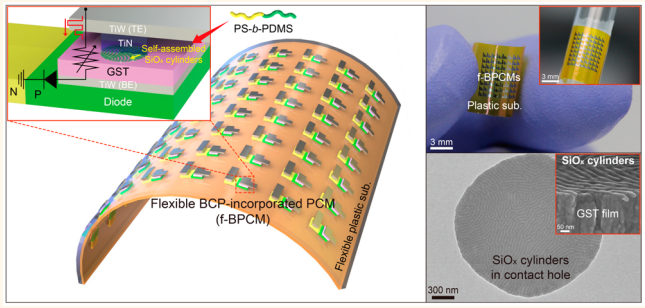
ABSTRACT Flexible memory is the fundamental component for data processing, storage, and radio frequency communication in flexible electronic systems. Among several emerging memory technologies, phase-change random-access memory (PRAM) is one of the strongest candidate for next-generation nonvolatile memories due to its remarkable merits of large cycling endurance, high speed, and excellent scalability. Although there are a few approaches for flexible phase-change memory (PCM), high reset current is the biggest obstacle for the practical operation of flexible PCM devices. In this paper, we report a flexible PCM realized by incorporating nanoinsulators derived from a Si-containing block copolymer (BCP) to significantly lower the operating current of the flexible memory formed on plastic substrate. The reduction of thermal stress by BCP nanostructures enables the reliable operation of flexible PCM devices integrated with ultrathin flexible diodes during more than 100 switching cycles and 1000 bending cycles.



KEYWORDS: flexible electronics · flexible memory · one diode-one resistor · phase change memory · block copolymers · self-assembly

Rapid advances in flexible electronics have been recently made for their potential use in paper-like displays,[1,2] plastic radio frequency identification (RFID) tags,[3] bioimplantable devices,[4−6] and other types of electronic devices.[7−11] To operate flexible electronic devices, however, further performance improvement of flexible memories is a key issue owing to their critical roles in code processing, data storage, and radio frequency communication.[12−15] Phase-change memory (PCM) is one of the most viable candidates for next-generation nonvolatile flexible memories due to its multiple advantages of excellent cycling endurance, high speed, and outstanding scalability.[16−18] In the realization of a high-performance flexible PCM, a large writing current is the major obstacle because flexible PCM devices work at a high current, for example, over 50 mA for micrometer contact.[19−21] The operating current of PCM can be diminished as the switching volume of the phase-change material becomes smaller (*i.e.*, a decrease in the power consumption per cell with reduction in device feature size).[22] Although a straightforward way to reduce writing current is to further decrease the contact area between the heater layer and the phase-change material, conventional photon-based nanolithography techniques cannot easily be applied on rough flexible substrates due to limit of high-precision focusing and inaccuracy of multilevel registration.[21] Furthermore, previously reported flexible phase-change memories, composed of nanodot/wire arrays, are not practical solutions for commercialization from the viewpoints of device reliability, nanomaterials alignment, and interconnection issues.[23,24]

Block copolymer (BCP) self-assembly, a spontaneous organization phenomenon of two mutually immiscible polymer blocks, can achieve regularly ordered arrays with sub-20 nm features.[25−32] Self-assembly of BCPs has shown promising potential to complement photolithography because of

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Received for review January 12, 2015 and accepted March 25, 2015.

Published online March 31, 2015
10.1021/acsnano.5b00230

its low-cost process, excellent resolution, scalability, and applicability to the conventional CMOS technology.[25,26,33−36] Moreover, Si-containing BCPs can be used as nanoinsulators that can modulate the performance of highly miniaturized memory devices,[32] and they can be applied in continuous nanomanufacturing technology for oriented flexible BCP thin films, such as roll-to-roll and jet printing process.[37,38] We also previously demonstrated considerable power reduction of PCM on a solid substrate by incorporating tailored silica nanostructures derived from the BCPs.[20]

Herein, we report the realization of a flexible one diode-one PCM (1D-1P) array that uses BCP self-assembly to lower the operating current of the memory formed on plastic substrates. The self-assembled SiO_x nanoarchitectures between the phase-change material and the heater layer effectively reduce the writing current of flexible PCMs by 4 times compared to conventional structures without BCP nanostructures. Our simulation results support the hypothesis that the flexible BCP-incorporated PCM (f-BPCM) can operate with sufficiently low power, making it compatible with polymer substrates due to current-blocking nanostructures derived from BCPs. We also suggest that this approach can be applied in a variety of cell sizes and technology nodes. Finally, we demonstrate the fabrication of flexible 1D-1P devices by integrating a switching element of ultrathin single-crystal Si diodes with an excellent forward current density (>10^5 A/cm^2) and rectifying ratio (>10^5) to prevent unintended current leakage paths between neighboring memory cells.[39] These results may open up a new opportunity for realizing flexible PRAM for practical electronic applications.

RESULTS AND DISCUSSION

Figure 1a shows a schematic illustration of the flexible PCM arrays on a plastic substrate. This flexible 1D-1P unit cell consists of an f-BPCM based on $Ge_2Sb_2Te_5$ (GST) and a single-crystal silicon diode as a selection element. Figure S1 in the Supporting Information describes the fabrication procedures of the 1D-1P devices. To reduce the reset current of the flexible PCM devices, the self-assembly of Si-containing poly(styrene-*b*-dimethylsiloxane) (PS-*b*-PDMS) BCPs was introduced because the operation current of conventional PCM device (contact hole size = 2 μm) on plastics is 58 mA, as shown in Supporting Information Figure S2, which not only thermally damage a plastic substrate and intercells but also exceeds the current supply capability of the selection device.[19,40−42] The thermally stable SiO_x nanostructures can easily be converted from self-assembled PDMS microdomains after O_2 plasma treatment,[27,29,43] as shown in the inset of Figure 1a. The regularly arranged insulating SiO_x nanostructures can be highly beneficial for reducing the contact area between GST and TiN films on plastics, thus resulting in a decrease in the reset current owing to the reduced switching volume. The flexible 1D-1P devices on a 25 μm-thick polyimide (PI) film ensure good flexibility without any mechanical damage on a glass rod or upon bending motions by fingers (Figure 1b). Figure 1c presents a photographic image of flexible 1D-1P unit cells on a plastic substrate. The inset of Figure 1c is a magnified optical micrograph of the marked area. The cross-sectional scanning electron microscopy (SEM) image of the f-BPCM confirms the successful formation of silicon oxide nanopatterns on the GST phase-change materials (Figure 1d). To form uniformly monolayered silica nanostructures on the GST thin film, the thickness of the initial BCP film was optimized to be about 35−40 nm. The final thickness of nanocylinders converted from the BCP film was measured to be ~20 nm as shown in the inset of the Figure 1d. In the present study, a cylinder PS-*b*-PDMS BCP was self-assembled for the formation of in-plane fingerprint-like nanopatterns confined to the circular contact hole of the PCM device, as shown in a top-view SEM image (Figure 1e). The inset image of Figure 1e also shows a magnified SEM image of 20 nm-width SiO_x cylinders with an area fill factor of 50%. These 2 μm contact holes play important roles in determining the contact area between GST and TiN films and also serve as a topographical template for the self-assembly patterns on flexible substrates.[28] Note that recent advances in the industrial roll-to-roll process have enabled 2 μm resolution of roll patterning for flexible displays; therefore, our directed self-assembly (DSA) of a 2 μm hole PCM device might be suitable for the roll-to-roll mass-production process.[44] Furthermore, the processing cost for solution-based BCP self-assembly is extremely low compared to conventional nanolithography techniques, and it can also be combined with roll-to-roll fabrication for large-area and high-throughput production.[37] The choice of this BCP morphology including dots, vertical cylinders, and perforated lamellae was motivated by control of the contact-area fill factor and the dependence of the reset current during switching operation.

To evaluate the performance enhancement of the f-BPCM device (Figure 2a), electrical tests were conducted using a semiconductor characterization system and a pulse generator. The f-BPCM was switched from the high resistance state (HRS, amorphous state) to the low resistance state (LRS, crystalline state) at ±3.5 V and 3.6 mA when the voltage pulse of 1 μs width was applied (SET operation). The resistance state of f-BPCM returned to the HRS at ±8.5 V and 14.9 mA when the voltage pulse of 140 ns width was applied (RESET operation). Operation speed of the f-BPCMs can be improved by applying a constant low voltage *via* prestructural ordering or by modifying the phase

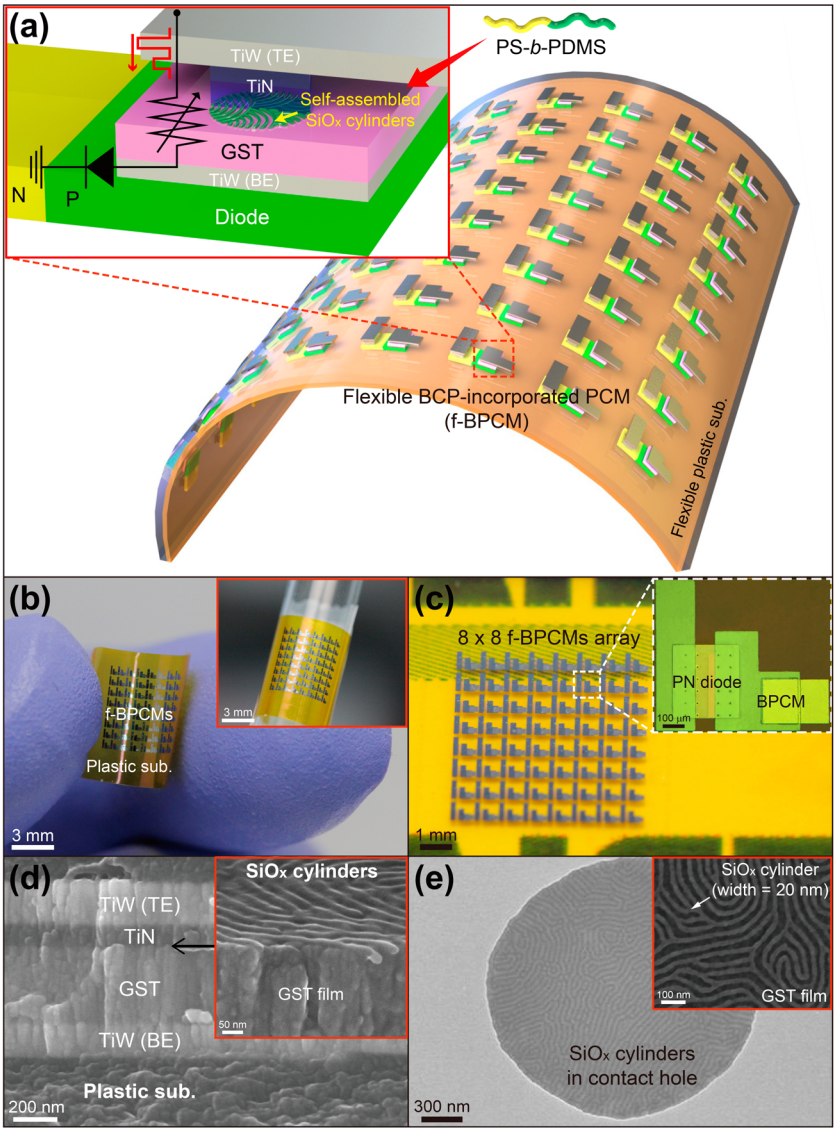

Figure 1. (a) Schematic of f-BPCM arrays with diodes on a plastic substrate. The inset image shows a device structure integrated with the single silicon diode and the PCM inserting SiO_x nanostructures. (b) Photograph of the f-BPCM cells with diodes on a 25 μm thick polyimide substrate. The inset shows the device wrapped on a glass rod with a diameter of 7 mm. (c) Photograph of f-BPCM cells integrated with diodes by an 8 $\times$ 8 array. The inset is a magnified optical image of the unit cell. (d) Cross-sectional SEM image of the f-BPCM device. The inset shows a tilted SEM image of self-assembled SiO_x nanostructures on GST thin films. (e) Top-view SEM image of the self-assembled SiO_x cylinders formed within 2 μm-diameter contact hole. The inset is a magnified SEM image of the SiO_x cylinders on GST thin films.

change materials.[45,46] Comparison of these switching characteristics to those of a conventional PCM structure on a plastic substrate shows that the RESET voltage and current of f-BPCM are remarkably reduced from 25 to 8.5 V and from 58 to 14.9 mA, respectively (Figure 2a and Supporting Information Figure S2). The decrease in RESET current is known to be due to the localized phase transition induced by employing SiO_x nanostructures at the interface between GST and TiN layers.[20] Moreover, this configuration of f-BPCM cells results in the reduction of switching thickness of the GST layer, which lowers SET voltage from 6.4 to 3.5 V (Figure 2a and Supporting Information Figure S2). It is because the SET voltage is proportional to the phase change line length of GST layer along the direction of applied voltage.[47,48] To confirm the effect of reducing operating current by incorporating the BCP self-assembled nanostructures into the contact hole, the f-BPCM devices were analytically simulated by the electrothermal method.[49] The nanopatterned silica layer with 50% coverage was adopted for the electrical and thermal isolation of the TiN and the GST region. The mathematical model for heat transfer by conduction in the f-BPCM cell is expressed as

$$\rho C \frac{\partial T}{\partial t} = Q + \nabla(k \nabla T) \quad (1)$$

where ρ is the density, C is the heat capacity, T is the temperature, t is the time, Q is the heat flux, and k is

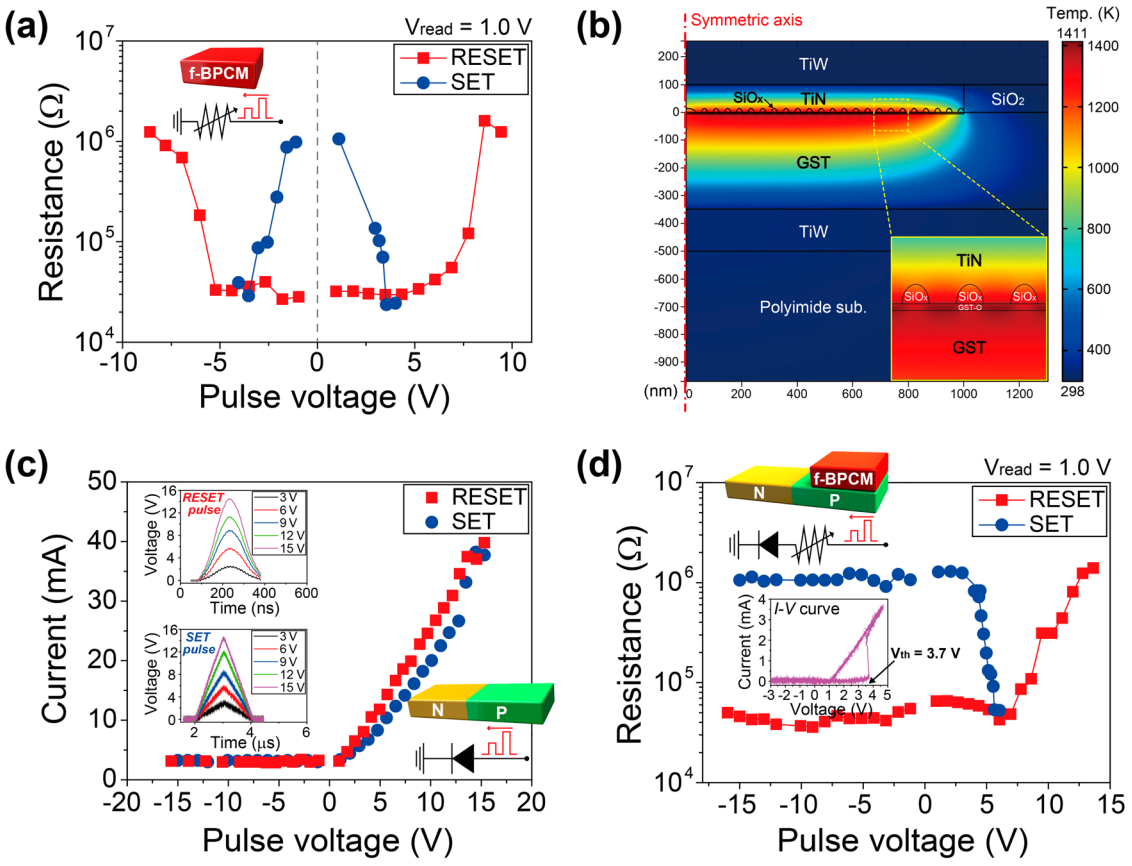

Figure 2. (a) $R-V$ curves and circuit diagram of the f-BPCM at the forward and reverse pulse voltage. (b) Temperature distributions calculated by electrothermal simulations for f-BPCM cell in the 2 μm contact hole when a current pulse of 15 mA was applied. (c) Current and pulse voltage characteristics and the related circuit diagram when RESET and SET voltage were applied to the flexible single crystal silicon diode with voltage pulses from −15 to 15 V. The inset shows detailed voltage waveforms for the RESET (140 ns) and SET (1 μs) processes. (d) $R-V$ curves of the flexible 1D-1P unit cell at the forward/reverse pulse voltage and the corresponding circuit diagram. The inset graph shows $I-V$ curves of the 1D-1P unit cell on the plastic substrate. The pulse widths for SET (solid blue circle) and RESET (solid red square) operations were set to be 1 μs and 140 ns, respectively.

the thermal conductivity.[50] The heat caused by Joule heating Q is described as

$$Q = J \cdot E = \sigma E^2 = \sigma |\nabla V|^2 \qquad (2)$$

where J is the electric current density, E is the electric field, σ is the electric conductivity, and V is the electric potential. As fundamental equations for the numerical simulation of f-BPCM devices, eqs 1 and 2 were solved by finite-element analysis with COMSOL multiphysics software. Equation 2 indicates that the Joule heating should mainly occur in the areas with high current density. The existence of the nanopatterned silica and oxidized top surface of the GST film (GST-O) after O_2 plasma treatment would result in enhancement of the current density in the region between the two adjoining nanopatterned insulators.[49] Moreover, the O-GST layer can induce the focusing of heat generation near the interface due to its much higher resistance compared to pristine GST. Therefore, the temperature distributions in the gaps between the adjacent silica nanoarchitectures are significantly modified as shown in the simulated temperature profile (Figure 2b). For the PCM cell with the nanopatterned silica, when a reset current pulse of 15 mA was applied with a pulse width of a 140 ns, the calculated maximum temperature of the GST film was 1411 K, which is sufficiently higher than the melting point of GST (T_{melt} = 888 K). As compared with simulation result of conventional flexible PCM device (Supporting Information Figure S3), in addition, the modified temperature profile by localized heating effects leads to relieve thermal stress of plastic substrate and heat disturbance among the adjacent cells during operation of a PCM device and a diode.

To prevent cell-to-cell interference in a cross-point-type array for high-density PRAM, flexible ultrathin silicon PN diodes were adopted. We measured the current-pulse voltage characteristics of the flexible single-crystal PN diodes of the selection device before their integration with f-BPCM cells (Figure 2c). The integrated diode exhibited high-performance electrical properties on plastics, including a threshold voltage of 0.7 V, a current density of 10^5 A/cm^2, and a high rectifying ratio of 10^5 at $\pm$1.0 V, at the forward bias (Supporting Information Figure S4). The N-region was grounded, and the applied voltage to the P-diode

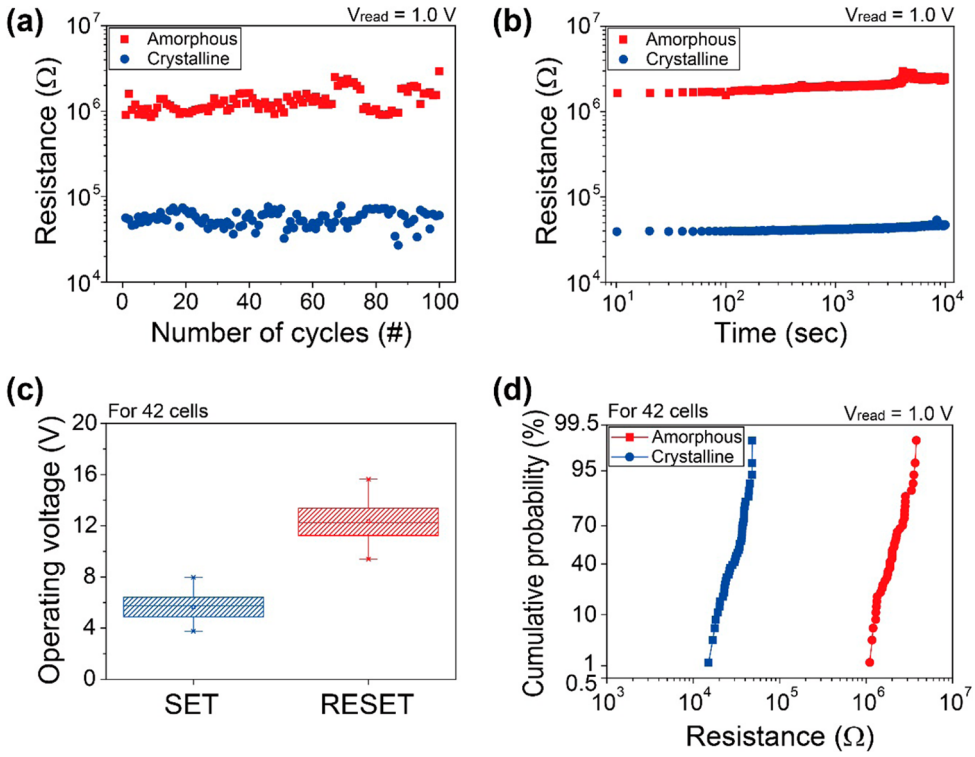

Figure 3. (a) Endurance characteristics of the flexible 1D-1P device during 100 repeated cycles. (b) Time retention test of the 1D-1P device on the plastic substrate. (c) SET and RESET voltage distributions of the flexible 1D-1P devices obtained from 42 different cells. (d) Cumulative probability of resistance state distributions from 42 different cells.

region was varied from −15 to 15 V in the pulse mode. Figure 2c indicates that the current output of selection diode was large enough to switch the f-BPCM because the forward diode current exceed the turn-on current of PCM devices with localized heating structure. It should be noted that the pulse current of the f-BPCM device measured from voltage pulse for RESET/SET operations (inset of Figure 2c) was effectively blocked at the reverse bias by the introduction of the intrinsic region between the P- and N-doping areas to keep the rectifying capability even at the high reverse voltage. Laterally structured PN diodes can be converted into high performance vertical diode structures by incorporation of well-controlled ion implantation or epitaxial silicon growth for high-density 1D-1P structures.[51−53] The *R*−*V* characteristics of the flexible 1D-1P unit cell in the pulse mode and the corresponding circuit diagram are shown in Figure 2d. The electrical properties of the 1D-1P unit cell were evaluated in conditions equivalent to those of the f-BPCM, and the resistance values were measured to be higher than those of the f-BPCM device without the diode. This phenomenon can be explained by the additional forward state resistance of the silicon diode. The f-BPCM integrated with a single-crystal silicon diode was successfully switched between the crystalline state and the amorphous state in the forward bias with the SET voltage of 5.6 V, RESET voltage of 12.8 V, and a resistance ratio of 20, while there was no switching behavior at the reverse bias in contrast with the *R*-*V* characteristics of the f-BPCM (Figure 2a) due to the rectifying property of the selection device. The *I*−*V* characteristics of the flexible 1D-1P unit cell shown in the inset of Figure 2d also support the fact that resistance switching was only observed in the forward bias. The experimental measurements demonstrate that the coupling of the f-BPCM with a flexible Si diode plays a critical role in diminishing the cell-to-cell interference without operating error.

Endurance and retention tests of the flexible 1D-1P devices were systematically performed. Figure 3a shows the resistance of the flexible 1D-1P devices in both amorphous and crystalline states with variation of the number of cycling endurance tests under repeated RESET/SET voltage pulses. Consistent resistance states were observed without significant decay during 100 repeated switching cycles. To confirm the data storage ability in the HRS and LRS, the retention characteristics of the flexible 1D-1P devices were investigated at the read voltage of 1.0 V as shown in Figure 3b. Our memory cell exhibited a stable retention property up to 10^4 s at room temperature, ensuring excellent reliability of the flexible 1D-1P devices on the plastic substrate. Although the ON/OFF resistance ratio of our flexible PCMs with and without nanoinsulators is lower than the typical values in literatures, it is considered to be a sufficient value required for practical resistive switching memory cells used in commercial applications.[54] To improve the resistance ratio of f-BPCMs, it would be effective to increase and optimize

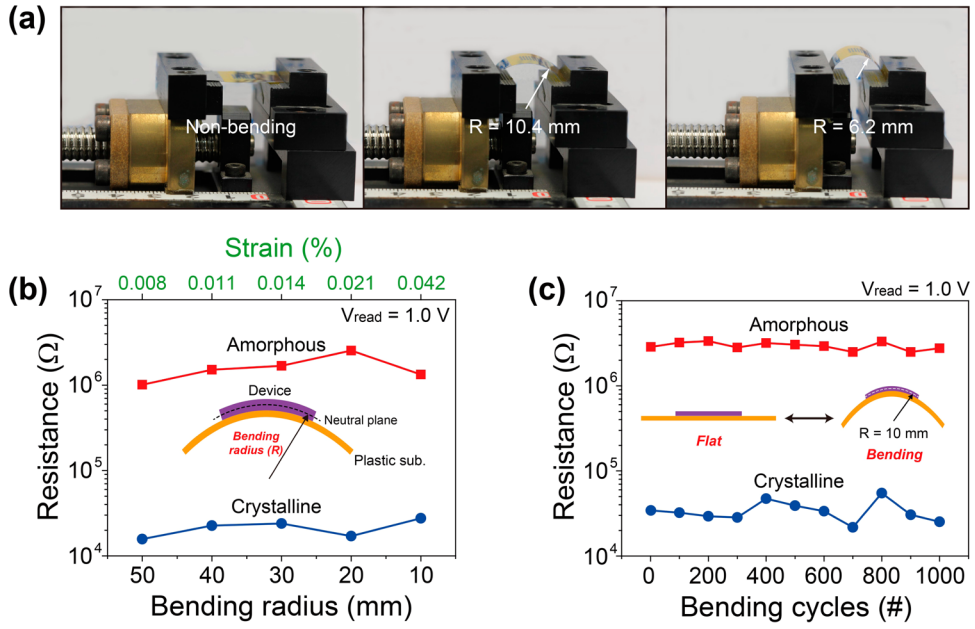

Figure 4. (a) Photograph of bending and unbending states. (b) Resistance ratio between amorphous and crystalline states and strain in GST films as a function of the bending radius. (c) Resistance ratio of the device during the 1000 repeated bending cycles with a 10 mm-bending radius.

the thickness of SiO_2 grown by plasma-enhanced chemical vapor deposition (PECVD) (See Supporting Information Figure S1c), which effectively lowers the leakage current.

To demonstrate the reproducibility of the flexible 1D-1P operation, 42 different cells were fabricated and analyzed statistically as shown in Figure 3c,d. For this particular data set, the yield of the integrated devices among the 8 × 8 memory array (64 in total) was about 66%. However, we strongly believe that the device yield can be improved further by applying automated fabrication processes.[37,55] A box-whisker plot obtained from the *R*−*V* curves of the flexible 1D-1P cells shows the SET and RESET voltage distributions (Figure 3c). Good uniformity during switching operations can be further confirmed by the cumulative probability of the resistance obtained from the *R*−*V* characteristic of 42 unit cells (Figure 3d). The ratio between HRS and LRS values was maintained without resistance overlap at the reading voltage of 1.0 V.

The mechanical bending tests were performed under various bending conditions on a bending stage machine to evaluate the mechanical reliability of the 1D-1P on a flexible substrate (Figure 4a). The flexible 1D-1P device was bent from a bending radius of 50 mm to that of 10 mm, and the resistance of amorphous and crystalline state was measured *in situ* (Figure 4b). The durability of the 1D-1P cell was measured through 1000 bending cycles at the fixed bending radius of 10 mm, as shown in Figure 4c. The resistance ratio between the HRS and LRS values of the 1D-1P was maintained without any significant change during the mechanical durability test. These results confirm that our flexible 1D-1P device is highly stable because presumably the entire device including self-assembled structures was fabricated at low temperatures below 300 °C, which is directly related to its compatibility with flexible electronic applications.[56]

For the theoretical analysis of the 1D-1P flexibility, the mechanics based on the calculated strains of our flexible phase-change materials was simulated as described below.[57] First, the distance between the neutral mechanical plane and the top surface can be computed as

$$h_{\text{neutral}} = \sum_{i=1}^{N} \bar{E}_i h_i \left(\sum_{j=1}^{i} h_j - \frac{h_i}{2} \right) \Big/ \sum_{i=1}^{N} \bar{E}_i h_i \qquad (3)$$

where N is the total number of layers, h_i is the thickness of the i^{th} layer (from the top), and $\bar{E}_i = E_i/(1 - v_i^2)$ can be calculated from the Young's modulus E_i and Poisson's ratio v_i of the i^{th} layer. The strain in the flexible 1D-1P devices is given by $\varepsilon = \gamma/R$, where R is the bending radius, and γ is the distance from the neutral mechanical plane. The physical data of our device materials used for calculating strain are provided in Supporting Information Table S1. The neutral mechanical plane is 4.5 μm below the top surface. The maximum distance from the GST thin film to the neutral mechanical plane is then 4.2 μm, which gives a strain of ~0.042% in the PCM devices for a bending radius R = 10 mm. Theoretical strains in GST films are calculated depending on the bending radius as shown in Figure 4b, which are much smaller than a crack-formed strain of 0.6% in previous experiment result.[58]

CONCLUSIONS

In conclusion, we introduced a novel methodology that shows how a bottom-up self-assembly based approach can realize a highly functional flexible

phase-change memory. BCP self-assembly was successfully adopted in the flexible PCM device to achieve significant approximately 4-fold current reduction. Our simulation results demonstrated that the use of self-assembled silica nanostructures effectively modulated the temperature distribution in flexible PCM devices. In addition, high-performance single-crystal diodes were integrated with the f-BPCM memory array as a switching element to solve the electrical interference between adjacent cells. Stable and reliable switching behaviors of the 1D-1P cell array were confirmed by the endurance/retention testing and the statistical analysis. The outstanding mechanical stability of the flexible 1D-1P device was demonstrated through bending fatigue testing as well as theoretical calculations. By combination with roll-based BCP patterning, our f-BPCM can be applied to cost-effective and universally mass-production line for flexible electronics.[37]

METHODS

F-BPCM Device Fabrication. The TiW bottom electrode (BE: 150 nm) and GST films (350 nm) deposited by direct-current (DC) sputter deposition were patterned on the anode region of the transferred P-doped Si membrane. Then, a 100 nm-thick SiO_2 insulator layer was grown by PECVD at 300 °C, and the contact holes with 2 μm diameter were patterned using i-line photolithography and subsequent reactive ion etching (RIE) with C_4F_8 gas, and the BCP self-assembly process was conducted. Lastly, TiN (100 nm) as a heating layer and TiW as the top electrode (TE: 200 nm) were deposited and photopatterned on the GST film.

BCP Self-Assembly Process. For easier and more uniform arrangement of the BCP microdomains on a rough flexible substrate, the GST surface was chemically modified with a hydroxyl-terminated homopolymer (PS−OH, the molecular weight = 38 kg/mol) brush layer by thermally treating the polymer at 150 °C for 2 h under vacuum. Then, a PS-*b*-PDMS BCP toluene solution was spin-coated. Physical values are listed as following: the molecular weight of PS-*b*-PDMS = 48 kg/mol, the PDMS volume fractions = 33.7%, Polymer Source Inc., concentration of 0.6 wt %, the polydispersity index of PS-*b*-PDMS = 1.18, the average molecular weight of PS and PDMS = 31.0 and 17.0 kg/mol, the glass transition temperatures of PS and PDMS = 103 and −125 °C. BCPs were self-assembled in the 2 μm diameter holes at room temperature under saturated toluene vapor (Supporting Information Figure S1d). The microphase-separated PDMS cylinders in a PS matrix were treated with CF_4 plasma (21 s at 50 W) followed by O_2 plasma (45 s at 60 W) using the RIE system, thus leading to formation of lying-down SiO_x nanocylinders. The incorporation of these organized SiO_x nanostructures into flexible PCM can be highly effective in reducing the power consumption.

Fabrication of Flexible Diode. Single-crystal silicon PN diodes doped at the elevated temperature of 1000 °C were fabricated on a silicon-on-insulator (SOI) wafer by a top-down lithographic technique and then transferred onto a flexible polyimide (PI, 25 μm thick, DuPont, Kapton) substrate using a PDMS stamp. Before PDMS stamping, poly(amic acid) (Sigma-Aldrich) was spin-casted onto a PI substrate and fully cured at 250 °C for 1 h to enhance adhesion between the PN diodes and PI substrate.

Device Measurements. All the electrical characterizations was performed at room temperature by using a Keithley 4200-SCS semiconductor measurement system equipped with a Keithley 4225-PMU pulse generator (waveform capture of current, voltage, and resistance), a 4225-RPM remote amplifier/switch, and a probe station.

Conflict of Interest: The authors declare no competing financial interest.

Acknowledgment. This work was supported by National Research Foundation (NRF) of Korea (grant code: NRF-2014R1A2A1A12067558) and Center for Integrated Smart Sensors as Global Frontier Project (CISS-2012M3A6A6054193 and CISS- 2011-0031848) funded by the Korea government (MSIP) through the National Research Foundation of Korea (NRF).

Supporting Information Available: This material is available free of charge *via* the Internet at http://pubs.acs.org.

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